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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,365	09/25/2003	Gregory Michael Nordstrom	ROC920030212US1	1856

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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,365	NORDSTROM ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1* is/are allowed.

6)☒ Claim(s) *2-4,8-11,14-17,21-25 and 28-31* is/are rejected.

7)☒ Claim(s) *5-7,12,13,18-20,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on December 15, 2005.

2. This application has been examined. Claims 1-31 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 8-11, 14-17, 21-25, 28-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pettey et al. (US No. 6,594,712) in view of Saeki et al. (US No. 5,581,787).

In regard to claims 2, 15, 30-31, Pettey et al. disclose a method of allocating memory addresses to a plurality of input/output (IO) resources coupled to a plurality of IO endpoints in a memory mapped IO fabric (see figure 1, col. 6, lines 20-39), the method comprising: determining a location in the memory mapped IO fabric for each IO endpoint among the plurality of endpoints (see col. 9, lines 44-65). But Pettey et al. do not specifically disclose non-uniformly allocating memory address ranges to the plurality of IO endpoints based upon the determined locations of the IO endpoints in the memory mapped IO fabric. However Saeki et al. disclose non-uniformly allocating memory address ranges to the plurality of IO endpoints based upon the determined locations of the IO endpoints in the memory mapped IO fabric (see col. 5, line 66 through col. 6, line 28) to provide less access time with much less probability in no response thus facilitating the process for

determining the system configuration and reducing the processing time. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Saeki et al. into the teachings of Pettey et al. because it would provide less access time with much less probability in no response thus facilitating the process for determining the system configuration and reducing the processing time

In regard to claims 3, 16, Saeki et al. disclose wherein determining the location and non-uniformly allocating memory address ranges are performed during initialization of the memory mapped IO fabric (see col. 5, line 66 through col. 6, line 28) to provide less access time with much less probability in no response thus facilitating the process for determining the system configuration and reducing the processing time. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Saeki et al. into the teachings of Pettey et al. because it would provide less access time with much less probability in no response thus facilitating the process for determining the system configuration and reducing the processing time

In regard to claims 4, 17, Saeki et al. disclose wherein determining the location and non-uniformly allocating memory address ranges are performed during initialization of a computer to which the memory mapped IO fabric is coupled (see col. 5, line 66 through col. 6, line 28) to provide less access time with much less probability in no response thus facilitating the process for determining the system configuration and reducing the processing time. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Saeki et al. into the

teachings of Pettey et al. because it would provide less access time with much less probability in no response thus facilitating the process for determining the system configuration and reducing the processing time

In regard to claims 8, 21, Pettey et al. disclose wherein the memory mapped IO fabric comprises a PCI-compatible fabric (see figure 1, col. 6, lines 15-29).

In regard to claims 9, 22, Pettey et al. disclose wherein the memory mapped IO fabric comprises at least one PCI-compatible bus, wherein at least a subset of IO endpoints are IO slots coupled to the PCI-compatible bus, and wherein the location of each IO slot is defined by a slot identifier for such IO slot on the PCI-compatible bus (see figure 1, col. 6, lines 15-65).

In regard to claims 10, 23, Pettey et al. disclose wherein the memory mapped IO fabric comprises a plurality of PCI-compatible buses, wherein at least a subset of IO endpoints are IO slots coupled to the plurality of PCI-compatible buses, and wherein the location of each IO slot is defined by a bus identifier for the PCI-compatible bus to which such IO slot is coupled, and a slot identifier for such IO slot on the PCI-compatible bus to which such IO slot is coupled (see figure 1, col. 6, lines 15-65).

In regard to claims 11, 24-25, Pettey et al. disclose wherein the memory mapped IO fabric comprises a plurality of IO enclosures, each IO enclosure including at least one PCI-compatible bus among the plurality of PCI-compatible buses, wherein determining the location of an IO endpoint comprises accessing configuration data associated with the IO enclosure within which such IO endpoint is disposed (see figure 1, col. 6, lines 15-55).

In regard to claims 14, 28, Pettey et al. disclose wherein the IO fabric includes at least one IO fabric element allowing connectivity to a subset of the

plurality of IO endpoints (see figure 1), and wherein the memory address ranges that would be allocated to IO resources coupled to each IO endpoint in the plurality of IO endpoints are determinable from a publication available prior to installation of IO resources in the subset of IO endpoints (see col. 9, lines 14-65).

In regard to claim 29, Pettey et al. disclose the plurality of IO resources and the memory mapped IO fabric (see figure 1).

Allowable Subject Matter

5. Claim 1 is allowed over the prior arts of records.

6. Claims 5-7, 12-13, 18-20, 26-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 1, 5, 6, 12, 18, 19, 26 are allowable over the prior art of record because the prior art cited in its entirety showed any motivation to combine any of the said prior arts which teach wherein determining the location and non-uniformly allocating memory address ranges are performed by a partition manager in the logically-partitioned computer (claims 5, 18); wherein allocating memory address ranges to the plurality of IO endpoints includes allocating differently sized memory address ranges to first and second IO endpoints having the same connector type (claims 1, 6, 19); wherein non-uniformly allocating memory address ranges to the plurality of IO endpoints includes allocating memory address ranges to a plurality of IO slots coupled to the PCI-compatible host bridge from the memory address range allocated to the PCI-compatible host bridge (claims 12, 26).

The remaining claims, not specifically mentioned, are allowed for the same rationale as set forth their dependent claims.

Response to Amendment

8. Applicant's amendment and arguments, see pages 1-18, filed on December 15, 2005, with respect to the rejections of claims 1-31 under 35USC102/103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Saeki et al.

Conclusion

9. Claim 1 is allowed. Claims 2-4, 8-11, 14-17, 21-25, 28-31 are rejected. Claims 5-7, 12-13, 18-20, 26-27 are objected.

10. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Bennett et al. (US No. 6,907,510) disclose a mapping of interconnect configuration space.

Garbus et al. (US No. 5,884,027) disclose an architecture for an I/O processor that integrates a PCI to PCI bridge.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supersor, John Cottingham can be reached on (571) 272-7079 or via e-mail addressed to john.cottingham@uspto.gov. The fax phone number for this Group is (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to **[raymond.phan@uspto.gov]**.

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet

Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

lnformation regarding the status of an application may be obtained from the Patent Application lnformation Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see hop://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

RP

Raymond Phan
March 4, 2006

JOHN R. COTTINGHAM
PRIMARY EXAMINER